# Exhibit C

[redacted]

**IN THE UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

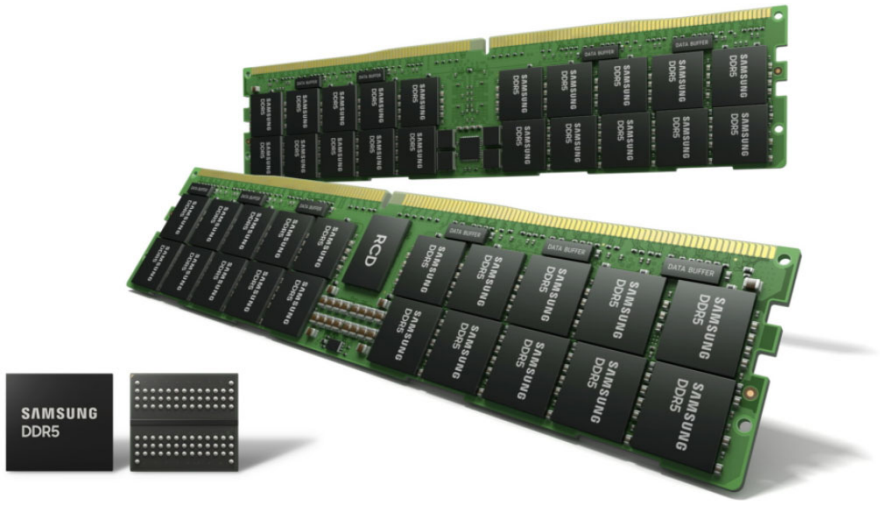
| | | |
|---|---|---|
| **NETLIST, INC.** | ) | |
| | ) | |
| Plaintiff, | ) | |
| | ) | |
| v. | ) | |
| | ) | |
| **SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC.** | ) | Civil Action No.2:21-cv-463 |
| | ) | |
| | ) | JURY TRIAL DEMANDED |
| Defendants. | ) | |

**COMPLAINT**

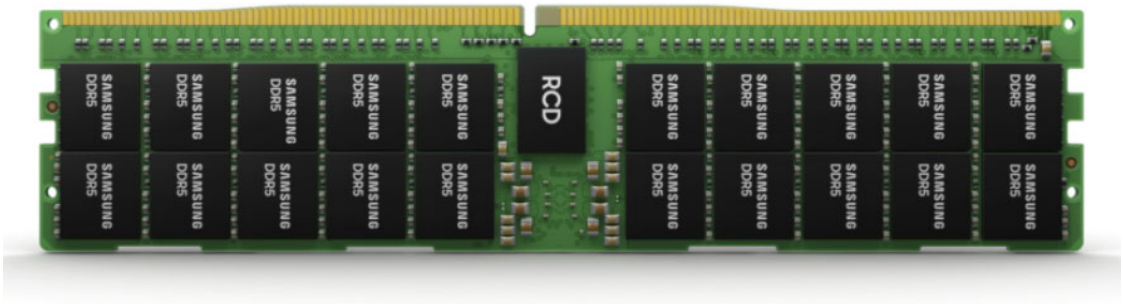
1. Plaintiff Netlist, Inc. ("Netlist"), by its undersigned counsel, for its Complaint against defendants Samsung Electronics Co., Ltd. ("SEC"), Samsung Electronics America, Inc. ("SEA"), and Samsung Semiconductor, Inc. ("SSI") (collectively, "Samsung" or "Defendants"), states as follows, with knowledge as to its own acts, and on information and belief as to the acts of others:

2. This action involves three of Netlist's patents: U.S. Patent Nos. 10,860,506 (the "'506 Patent," Ex. 1), 10,949,339 (the "'339 Patent," Ex. 2), and 11,016,918 (the "'918 Patent," Ex. 3) (collectively, the "Patents-in-Suit").

38. As further example, the Accused Instrumentalities include, without limitation, any Samsung DDR5 LRDIMM and DDR5 RDIMM products made, sold, used and/or imported into the United States by Samsung that are JEDEC-standard compliant memory modules. By way of non-limiting example, the accused DDR5 LRDIMM and DDR5 RDIMM products include products marketed and publicized in an October 12, 2021 Samsung Press release, as shown below.




Ex. 5 at 1 (depiction of a Samsung DDR5 LRDIMM).




*Id.* at 3 (depiction of a Samsung DDR5 RDIMM).

## IV. FIRST CLAIM FOR RELIEF – '506 PATENT

39. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

40. On information and belief, Samsung directly infringed and is currently infringing at least one claim of the '506 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example, and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '506 Patent.[1]

41. For example, to the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus. As an example, Samsung's website markets and contains datasheets for the accused DDR4 LRDIMMs.

**LRDIMM**

**Load Reduced DIMM**

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

42. Ex. 6 at 2 (depiction of a Samsung DDR4 LRDIMM). Each LRDIMM includes "a register for enhancing clock, command and control signals" as well as data buffers for "[e]nhanced

[1] The theories set forth herein are based on Netlist's present understanding of the Samsung Accused Instrumentalities. Netlist reserves the right to supplement or amend these contentions as permitted by the Local Rules and any Orders of the Court as discovery progresses. Further, Netlist's contentions contain images and examples illustrating Netlist's infringement theories. As such, the images and examples are not intended, and should not be read, as narrowing or limiting the scope of these contentions.

data signal." *Id.* It communicates with a server's memory controller via control and address signal lines in a memory bus as well as a data bus. For example:

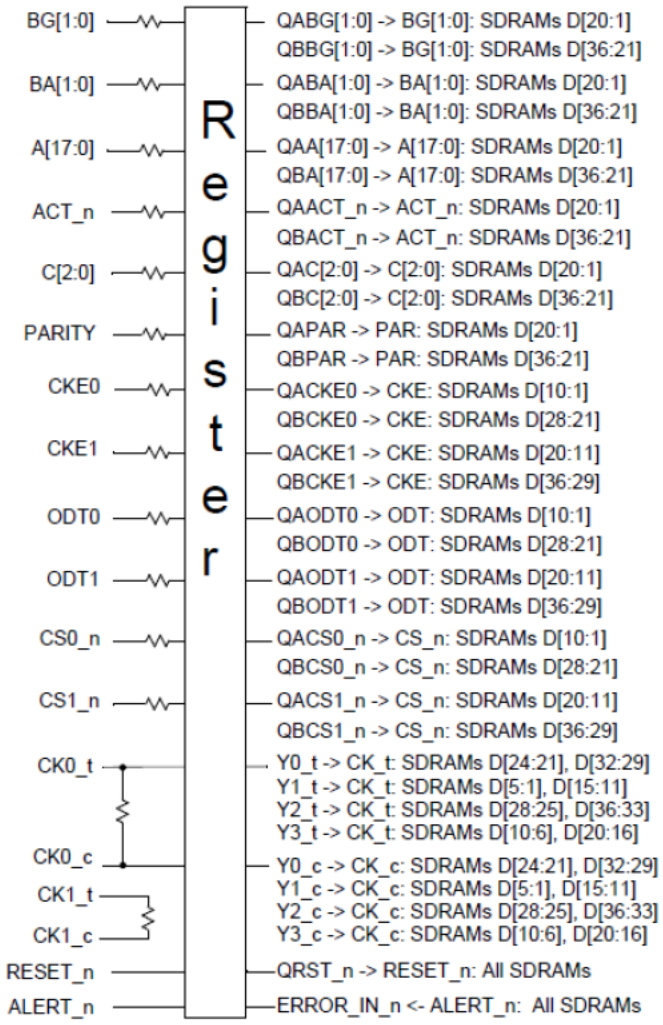
Load Reduced DIMM datasheet Rev. 1.4 DDR4 SDRAM

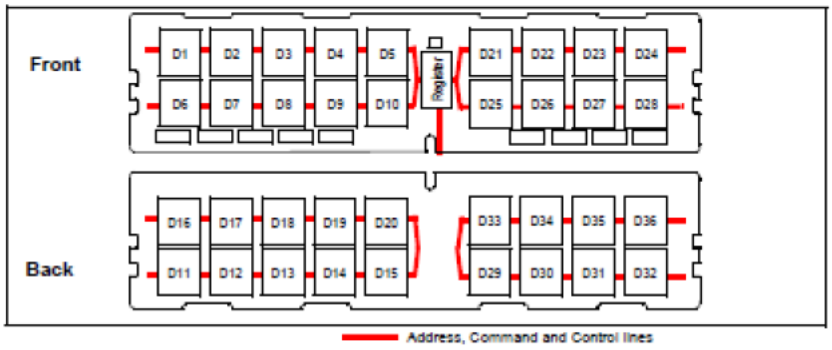
## 5. Pin Description

| Pin Name | Description | Pin Name | Description |
|---|---|---|---|
| A0–A17[1] | Register address input | SCL | I2C serial bus clock for SPD/TS and register |
| BA0, BA1 | Register bank select input | SDA | I2C serial bus data line for SPD/TS and register |
| BG0, BG1 | Register bank group select input | SA0–SA2 | I2C slave address select for SPD/TS and register |
| RAS_n[2] | Register row address strobe input | PAR | Register parity input |
| CAS_n[3] | Register column address strobe input | VDD | SDRAM core power supply |
| WE_n[4] | Register write enable input | VPP | SDRAM activating power supply |
| CS0_n, CS1_n, CS2_n, CS3_n | DIMM Rank Select Lines input | VREFCA | SDRAM command/address reference supply |
| CKE0, CKE1 | Register clock enable lines input | VSS | Power supply return (ground) |
| ODT0, ODT1 | Register on-die termination control lines input | VDDSPD | Serial SPD/TS positive power supply |
| ACT_n | Register input for activate input | ALERT_n | Register ALERT_n output |
| DQ0–DQ63 | DIMM memory data bus | RESET_n | Set Register and SDRAMs to a Known State |
| CB0–CB7 | DIMM ECC check bits | EVENT_n | SPD signals a thermal event has occurred |
| DQS0_t–DQS17_t | Data Buffer data strobes (positive line of differential pair) | VTT | SDRAM I/O termination supply |
| DQS0_c–DQS17_c | Data Buffer data strobes (negative line of differential pair) | RFU | Reserved for future use |
| CK0_t, CK1_t | Register clock input (positive line of differential pair) | | |
| CK0_c, CK1_c | Register clocks input (negative line of differential pair) | | |

NOTE :
1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Ex. 7 (M386AAK40B40 Datasheet) at 6.




NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.



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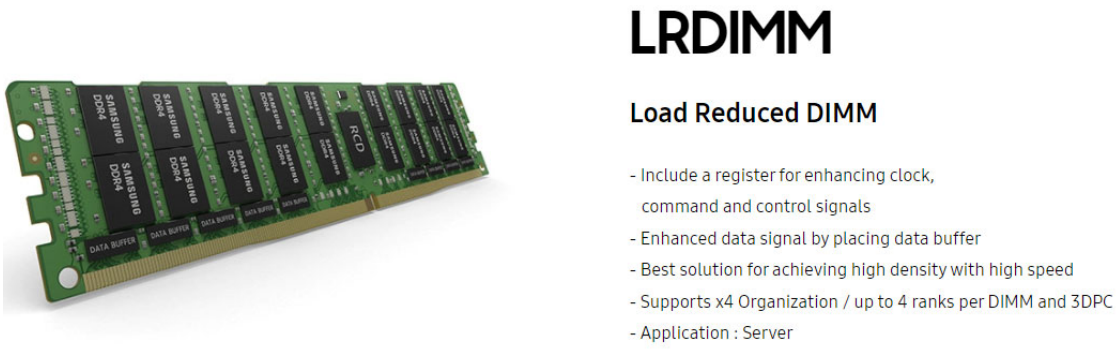
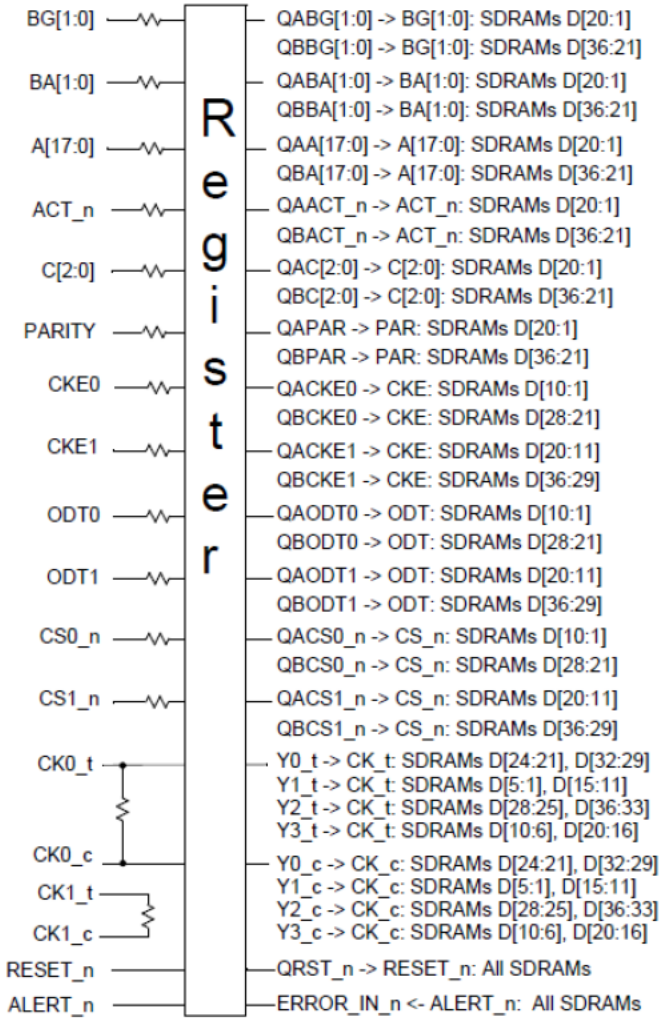
*Id.* at 10 (red lines in original).

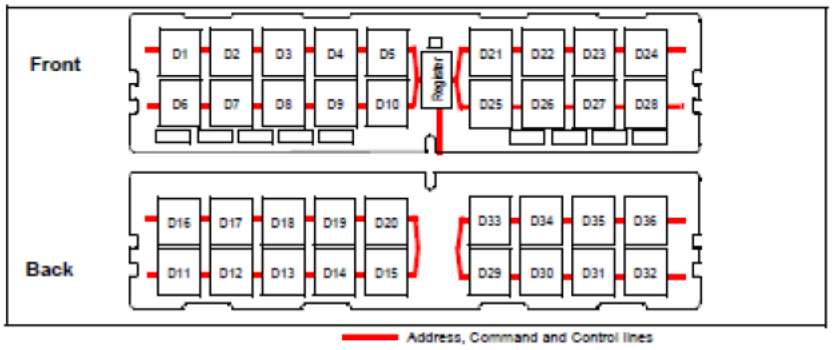
43. The accused DDR4 LRDIMMs further each comprise a module board having edge connections to be coupled to respective signal lines in the memory bus, as illustrated in the examples below.




Ex. 6 at 2 (depiction of a Samsung DDR4 LRDIMM); *see also* Ex. 7 (M386AAK40B40 Datasheet) at 42.

44. The accused DDR4 LRDIMMs further each comprise a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals, as illustrated in the example below.




NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.



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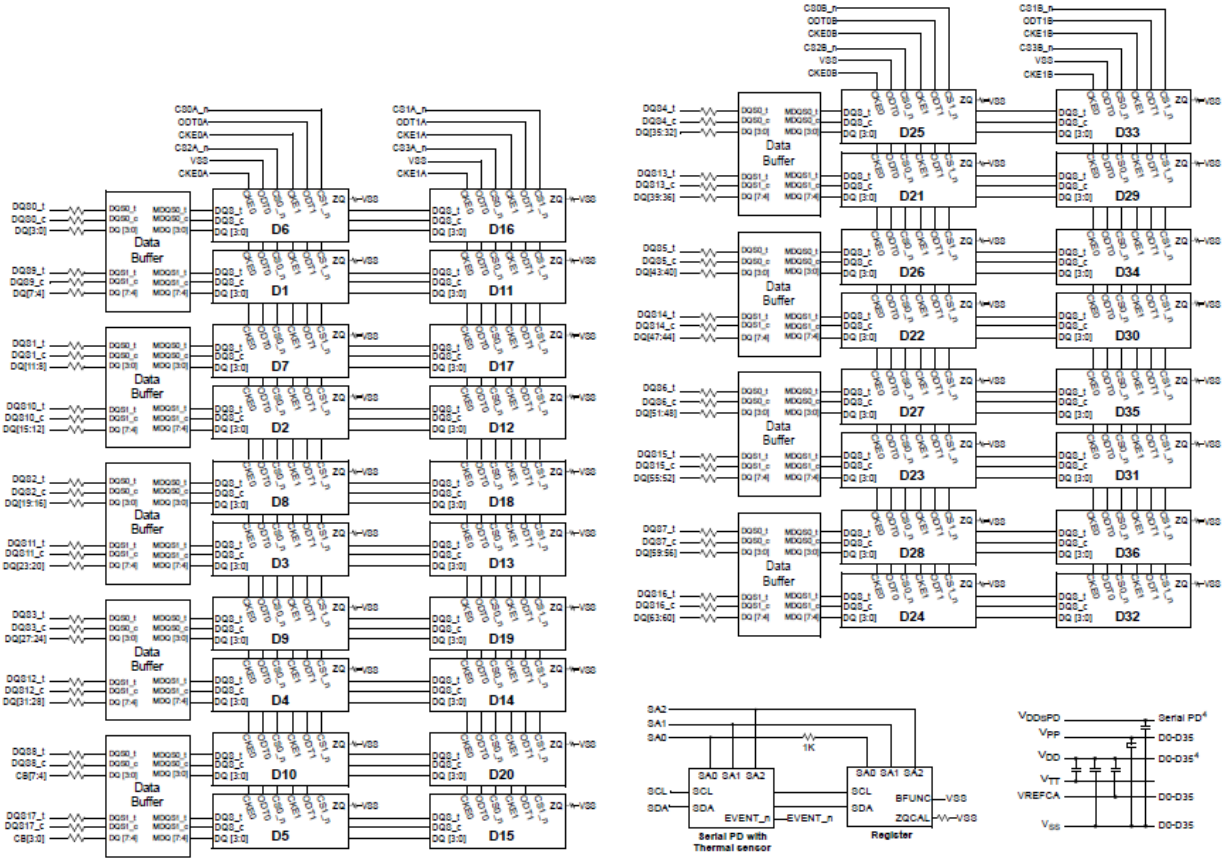
Ex. 7 (M386AAK40B40 Datasheet) at 10; *see also id.* at 42.

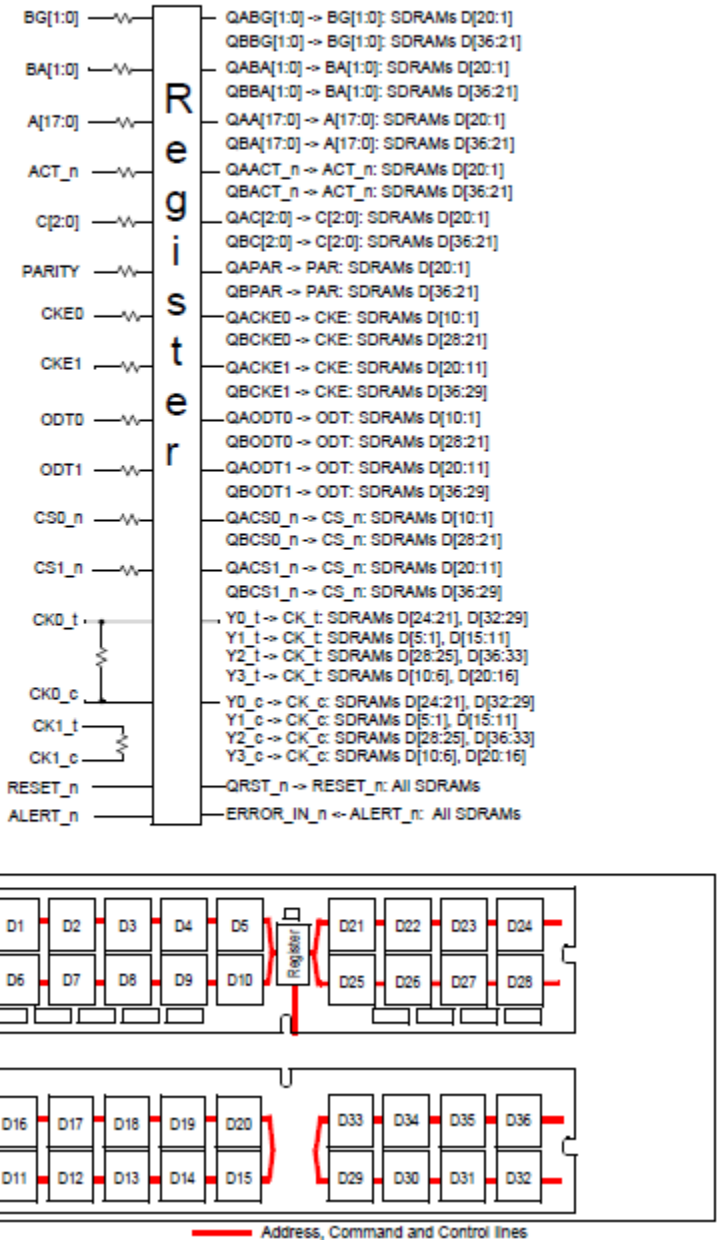


*Id.* at 11-12.

45. The accused DDR4 LRDIMMs also each include memory devices arranged in multiple ranks on the module board and coupled to the module control device (*e.g.*, RCD) via module C/A signal lines that conduct the registered C/A signals, as illustrated in the examples below.

### 9.1 128GB, 16Gx72 Module

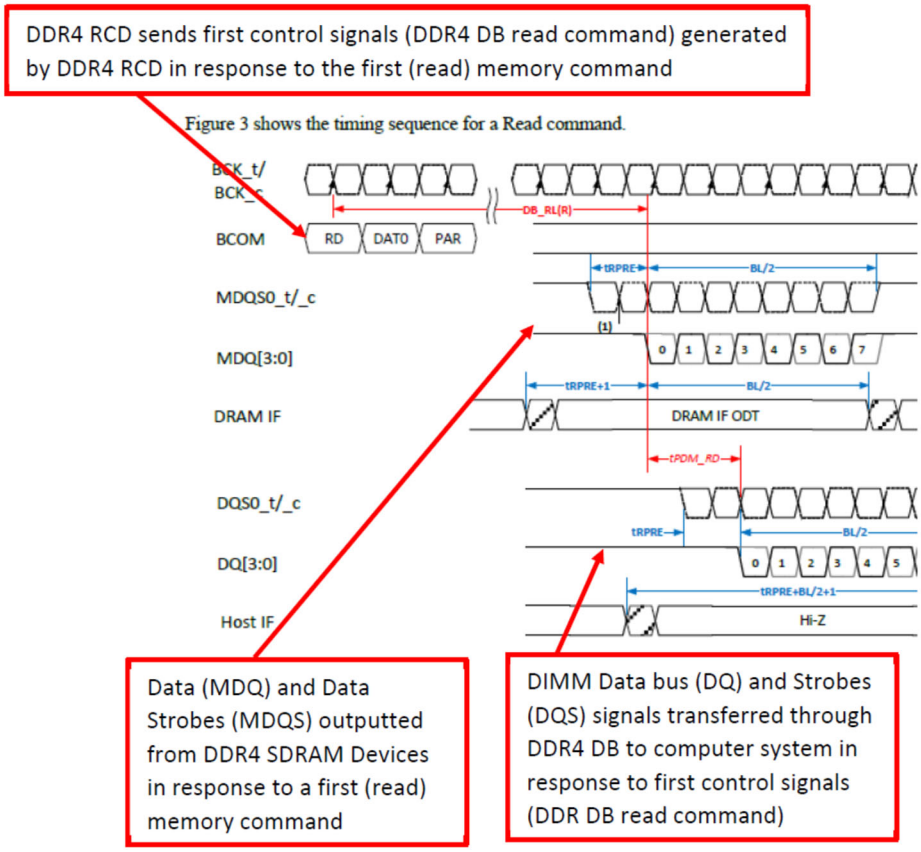
### (Populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAM



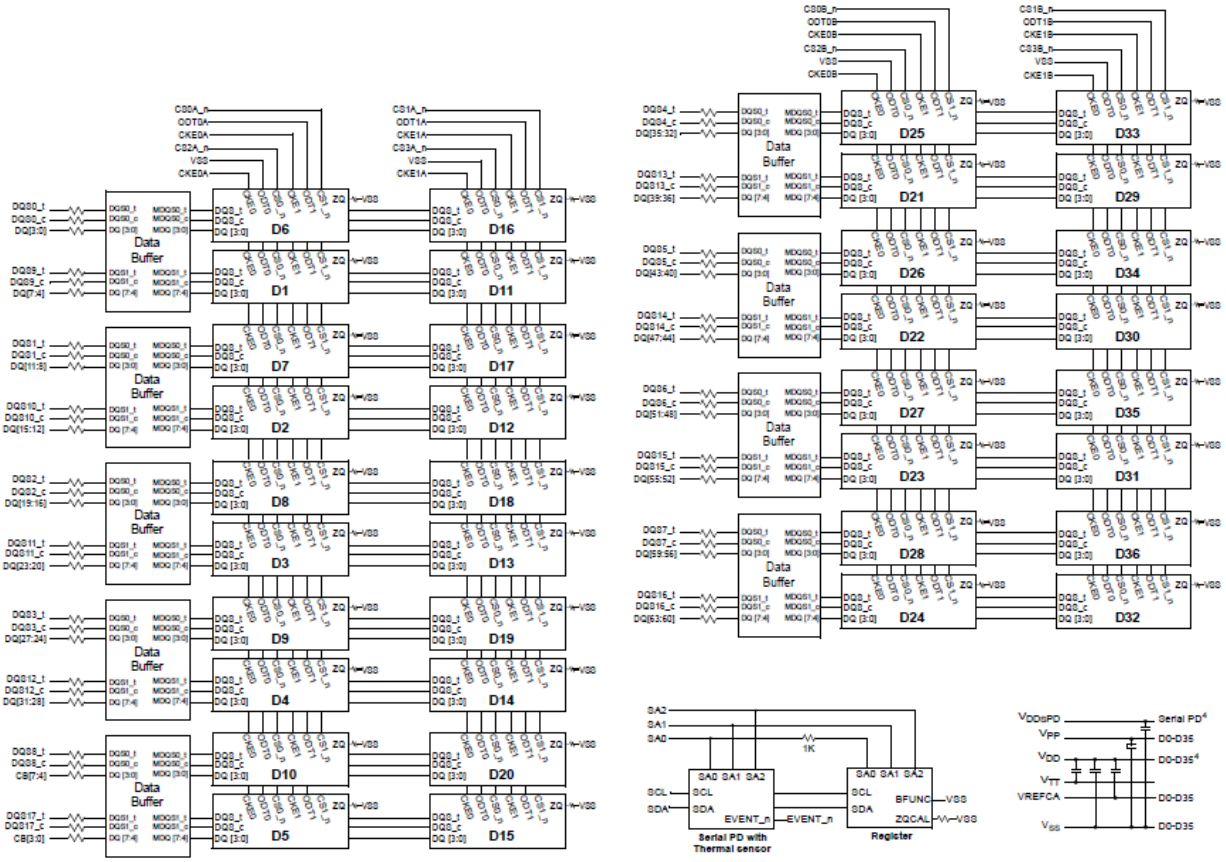

*Id.* at 10; *see also id.* at 42.

46. In each accused DDR4 LRDIMM's memory devices, the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a

first read strobe. For example, each accused DDR4 LRDIMM follows the timing sequence for a READ command shown below.



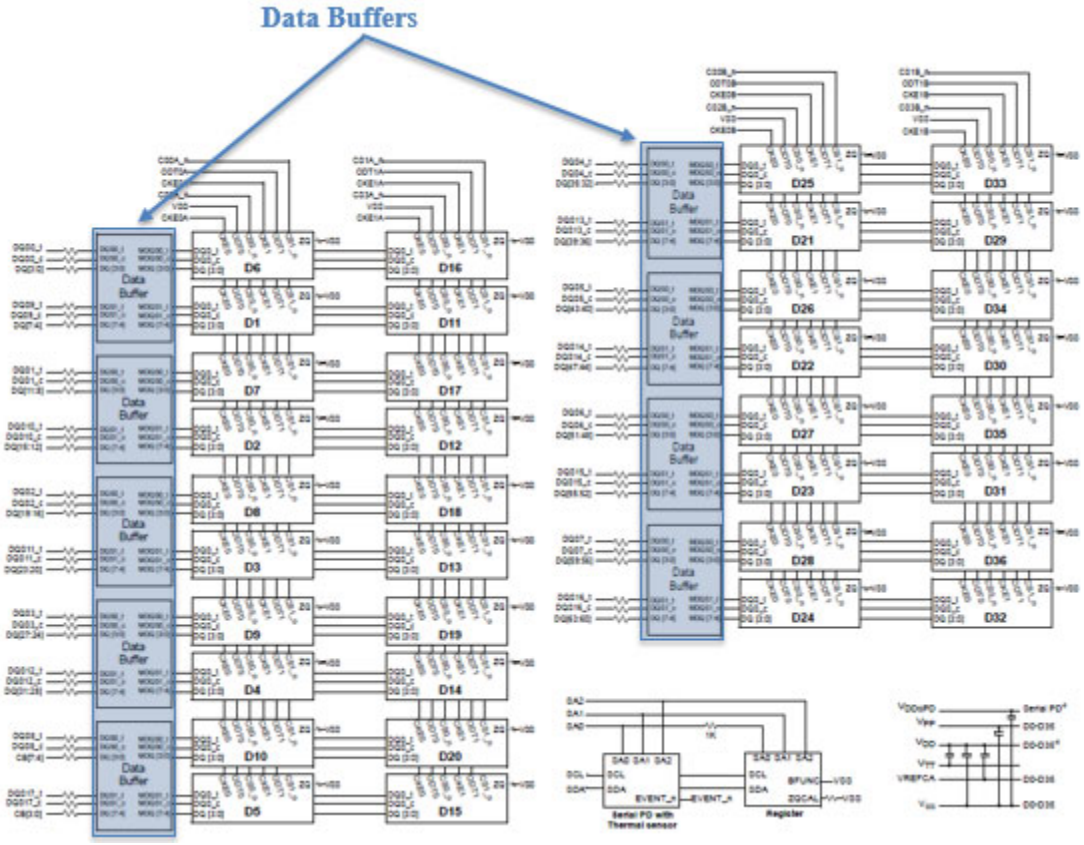

Ex. 9 (JEDEC JESD82-32A Standard), at 14 (annotated); *see also*, *e.g.*, Ex. 8 (M386A8K40BM1 Datasheet) at 11-12 (functional block for a representative product).




Ex. 8 (M386A8K40BM1 Datasheet) at 11-12.

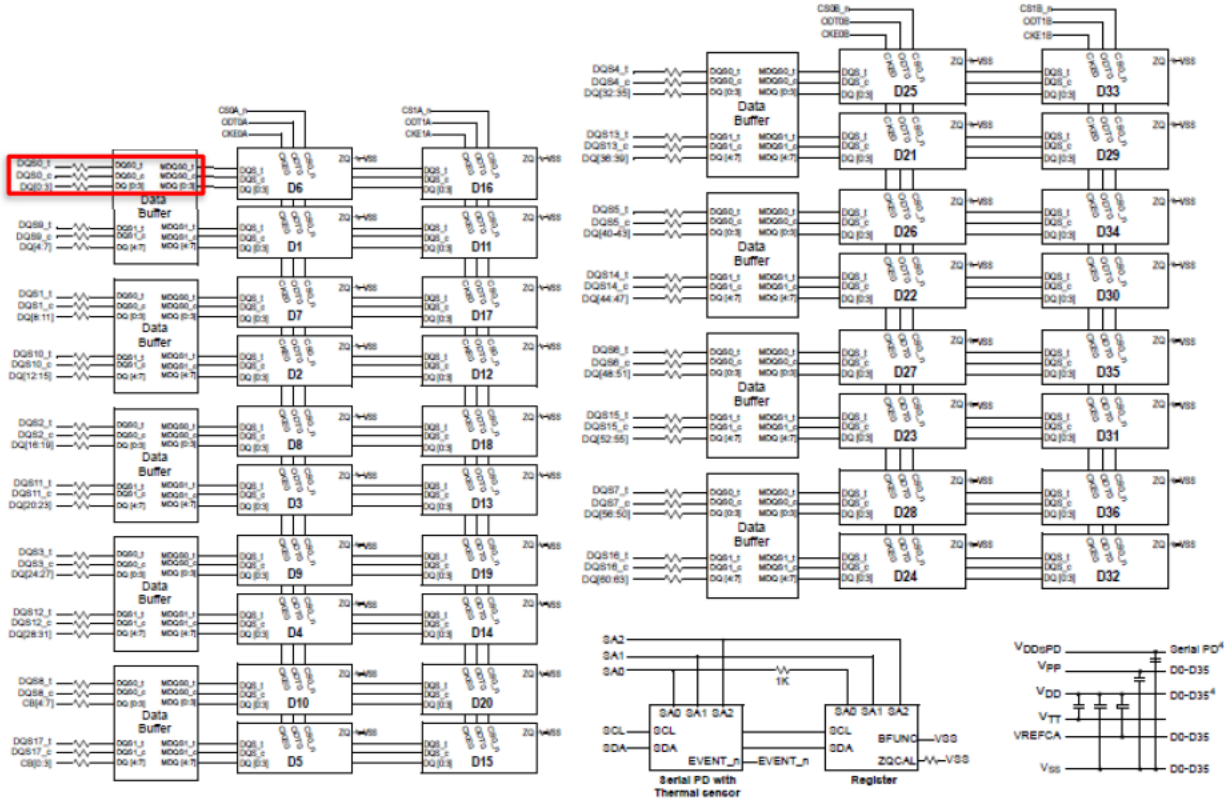
47. The accused DDR4 LRDIMMs further each include data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, as illustrated below.


Ex. 6 at 2 (depiction of a Samsung DDR4 LRDIMM).




Ex. 8 (M386A8K40BM1 Datasheet) at 11-12 (annotated to illustrate data buffers coupled between the plurality of 72-bit wide ranks and the 72-bit wide data bus).

48. In each accused DDR4 LRDIMM, a first data buffer on the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals: delay the first read strobe by a first predetermined amount to generate a first delayed read strobe; sample the first section of the read data using the first delayed read strobe; and transmit the first section of the read data to a first section of the data bus; wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations. For example, the strobes MDQSO_t and MDQSO_c are delayed by a variable delay circuitry and produce DQS0_t, DQS1_t and DQS0_c, DQS1_c. The predetermined amount of delay is determined based on training.




Ex. 7 (M386AAK40B40 Datasheet) at 11-12.

49. On information and belief, Samsung also indirectly infringes the '506 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung's customers and end users, in this District and elsewhere in the United States. For example, on information

and belief, Samsung has induced, and currently induces, the infringement of the '506 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM and other materially similar products that infringe the '506 Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

50. On information and belief, Samsung also indirectly infringes the '506 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung's customers and end-users infringement of the '506 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM and other materially similar products that infringe the '506 Patent. On information and belief, the accused DDR4 LRDIMM products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR4 LRDIMM and other materially similar products would be covered by one or more claims of the '506 Patents. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM and other materially similar products infringes at least one claim of the '506 Patent.

51. Samsung's infringement of the '506 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the '506 Patent since at least August 2, 2021. Samsung's infringement of the '506 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement,